In the Specification

At page 5, line 4, please replace "87" with --81--.

In the Abstract

Please amend the Abstract, a cleaned-up version of which is attached as Attachment A beginning at page i and a marked-up version as Attachment B beginning at page ii.

REMARKS

Responsive to the Office Action mailed April 25, 2002, the Examiner's comments and cited art have been studied. In view of the following remarks, the application is submitted as being in condition for allowance.

Amendments

As reflected above, the specification was amended to correct a reference numeral designation. Further, certain portions of the abstract were deleted to reduce the abstract to less than 150 words. In addition, the title was amended to be more descriptive.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-5, 7, 34-37 and 39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Swan, U.S. Patent No. 6,304,297. Applicants respectfully traverse these rejections.

Claims 1-5 and 7

Regarding claims 1-5 and 7, Swan fails to disclose transmitting outgoing digital television data to a display device when a programmed position of the display device is refreshed. Instead, Swan is directed to manipulating the display update rate[1] of video signals to minimize the adverse visual effects caused by adding or deleting frames.[2] As opposed to controlling when data is transmitted from its frame buffer, Swan monitors the display update rate and the refresh rate and repeats or skips frames at the "appropriate" times.[3] In Swan, the previously stored frame field of video data 28 is read from a front section 32 of frame buffer 14 as the current frame/field of video data 28 is being written

[1] Swan defines the "display update rate" as "the rate at which the image data is received." Col. 1, lns. 36-39.
[2] Col. 2, lns. 24-27.
[3] Col. 3, ln. 63–Col. 4, ln. 28.

into the back section 30 of frame buffer 14.[4] As such, transmitting the video data out of the front section 32 of frame buffer 14 is not based on when a programmed position of a display device is refreshed. Further, Swan's monitoring of the refresh rate 40 is different from determining when a "programmed position of [a] display device is refreshed."

Column 3, lines 15-16 and 19-23 of Swan, which are relied upon by the Office Action, describe the circumstance in which the display update rate and the refresh rate match. Such a match does not mean that the outgoing video data in Swan is transmitted based on when a programmed position of a display device is refreshed. A basic point is that the Office Action assumes that the display update rate must be based on the refresh rate for the rates to match. To the contrary, Swan just notes the possibility that the rates may match, hence the use of the term "[i]f" and the subsequent discussion in column 3, lines 25-28 of the circumstance when the rates do not match.

Claims 34-37 and 39

Regarding claims 34-37 and 39, Swan fails to disclose a "transmitting means for transmitting the outgoing digital television data in a storing means to the display device when a program position of the display device is refreshed" for the same reasons as explained above with respect to claims 1-5 and 7.

Claims 7 and 39

Regarding claims 7 and 39, Swan fails to disclose a refresh rate of incoming digital television data "decoupled" from a refresh rate of outgoing digital television data. In Swan, a need value module 22 monitors the display update rate 38 and refresh rate 40 and generates a need value indicating the need for the addition or dropping of a frame.[5] The need value is received by a manipulation module 24 which generates a manipulation display update rate signal 42.[6] Based on the manipulation display update rate signal 42, the manipulation module 24 may cause the video processor 12 or the display driver 16 to repeat or skip a frame.[7] Since Swan manipulates the display update rate 38 based in part on the refresh rate 40, the display update rate 38 and the refresh rate 40 are not "decoupled." Claims 7 and 39 are submitted to be allowable for these additional reasons.

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[4] Col. 3, lns. 1-4.

[5] Col. 3, ln. 63–Col. 4, ln. 1. Note these lines in Swan which are relied upon in the Office Action propose the monitoring of the display update rate 38 and refresh rate 40. That these rates are two different signals does not mean the rates are decoupled, especially given the role of the manipulation module 24 as discussed above.

[6] Col. 4, lns. 9-12.

[7] Col. 4, lns. 12-22.

Claims 57-61

Claims 57-61 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wilson et al., U.S. Patent No. 6,037,981. These rejections are respectfully traversed.

Regarding claims 57-61, Wilson fails to disclose a "graphics controller for receiving the decoded digital television data over a local bus from the digital television/local bus interface logic" or a "digital television/local bus interface logic for passing decoded digital television data." Wilson is directed to using a digital television as a remote display for a computer system.[8] The graphics controller 113 in Wilson is described as interfacing to a display device for "displaying images rendered or otherwise processed by the graphics controller 113 to a user."[9] Aside from the graphics controller 113 having nothing to do with television data, the Office Action misses the point that television data in Wilson is received at a digital television 200, not a computer system 212. In other words, the computer system 212 is transmitting television data to the digital television 200, not the other way around. For these fundamental reasons, Wilson fails to disclose a graphics controller for receiving decoded digital television data.

The Office Action relies upon the first I/O bus 112 of the computer system of Figure 1 of Wilson as disclosing "digital television/local bus interface logic passing decoded digital television data."[10] One problem with this Office Action position is that the television data in Wilson is still encoded—not decoded—when in the computer system 212. Figure 2 of Wilson shows that the television data is compressed before being provided to the transmitter 210. Figure 2 also shows that the receiver 202 is part of the digital television 200. As such, the television data is not decoded until it reaches the digital television 200.

Claim Rejections Under 35 U.S.C. § 103

Claims 6, 8-33, 38, and 48-56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Swan, U.S. Patent No. 6,304,297 and the Admitted Prior Art (APA) of Applicants' Figure 1. Applicants respectfully traverse these rejections.

Claims 8-24

Claims 8-24 are distinguishable from Swan and APA on a number of grounds. First of all, Swan and APA fail to teach or suggest the first frame buffer and second frame

[8] Col. 1, lns. 63-65.
[9] Col. 3, lns. 65–Col. 4, ln. 1.
[10] Paper No. 8, p. 7.

buffer which store incoming digital television data and outgoing digital television data in an alternating manner. The Office Action relies upon Swan as teaching this aspect, yet Swan maintains incoming video data in the back section 3 of frame buffer 14 and maintains outgoing video data in the front section 32 of the frame buffer 14.[11] The roles of the back section 30 and the front section 32 in Swan do not change. Stated another way, there is no suggestion in Swan to alternate maintaining the incoming video data between the back section 30 and the front section 32 or to alternate maintaining the outgoing video data between the front section 32 and the back section 30. For this reason alone, claims 8-24 are allowable.

Secondly, regarding claims 8-24, Swan and APA[12] fail to teach or suggest a "memory controller for storing the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer." Swan provides no suggestion that its "double buffering"[13] is controlled by a memory controller, much less a memory controller of "digital television/local bus interface logic." In Swan, the video processor 12 writes video data to the back section 30 of the frame buffer 14 and the display driver 16 reads video data from the front section 32 of the frame buffer 14.[14] This provides no suggestion of the claimed memory controller. Moreover, in characterizing the video processor 12 in Swan as the claimed memory controller, the Office Action ignores the fact that the display driver 16—not the video processor 12—reads video data from the front section 32 of the frame buffer 14.

Further regarding claims 8-24, Swan and APA fail to teach or suggest "digital television/local bus interface logic." Applicants' Figure 1 (APA), a prior art figure, relates to analog television data, not digital television data. As for Swan, the reference focuses on video graphics circuitry of a computer system[15] without offering any teaching regarding digital television or a local bus.

Claims 25-33

Regarding claims 25-33, Swan and APA fail to teach or suggest a "controller means for storing the incoming digital television data to one buffer means and reading the outgoing digital television data from another buffer means." As explained above, the "double buffering" in Swan instead involves the video processor 12 and the display driver

[11] Col. 3, lns. 1-4.
[12] Applicants' Figure 1, of course, does not show a memory controller.
[13] Col. 3, lns. 4-7.
[14] Col. 3, lns. 28-35.

16. As also explained above, Applicants' Figure 1 relates to analog television data, not digital television data. Thus, even if Swan and APA are combined, the combined teaching falls short of suggesting Applicants' controller means.

Further regarding claims 25-33, Swan and APA fail to teach or suggest the clamed "first buffer means" and "second buffer means." As explained above, Swan provides no suggestion to alternate storing incoming video data and outgoing video data between buffers.

Claims 48-52

Regarding claims 48-52, Swan and APA fail to teach or suggest the claimed "first frame buffer," "second frame buffer," "third frame buffer" and "fourth frame buffer" in at least two respects. For one, each of the claimed buffers stores an incoming data stream and an outgoing data stream "in an alternating manner." As explained above, Swan fails to teach or suggest a frame buffer that stores incoming data and outgoing data in an alternating manner.

The second distinction is Swan's failure to address multiple incoming data streams and multiple outgoing data streams. Claims 48-52 explicitly recite "a first incoming digital television data stream," "a second incoming digital television data stream," "a first outgoing digital television data stream" and "a second outgoing digital television data stream." The mention in Swan of "triple buffering" and "quadruple buffering"[16] does not teach or suggest multiple outgoing data streams or multiple incoming data streams. Note the frame buffer 14 in Swan having two sections (front section 32 and back section 30) involves a single path of incoming video data and a single path of outgoing video data.

Further regarding claims 48-52, Swan and APA fail to teach or suggest the recited memory controller. As explained above, the timing of when outgoing video data is read from the front section 32 of the frame buffer 14 depends on when incoming video data is written into the back section 30 of the frame buffer 14, not which portion of a display device is being refreshed. Further, causing the display driver 16 in Swan to repeat or skip a frame in providing outgoing video data to a display device is plainly different from controlling when outgoing video data is transmitted to a display device. Note Applicants' claimed memory controller is recited as "transmitting the first outgoing digital television data stream to the display device on a second portion of the refresh of the display device"

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[15] Col. 1, lns. 6-12.
[16] Col. 3, lns. 7-11.

and "transmitting the second outgoing digital television data stream to the display device on the second portion of the refresh of the display device."

Claims 53-56

Regarding claims 53-56, Swan and APA fail to teach or suggest "sending the decoded digital television data from a local bus of the computer system." Swan states that the "video processing module 12 may include a television decoder, such that the video graphics circuit 10 may receive video data 26."[17] Swan, however, fails to suggest that the video data is received over a local bus of a computer system. Applicants' APA does not fill this gap in Swan. That is, as explained in detail in Applicants' Specification, the computer system C of the APA relates to analog television data—not digital television data, and even the path of analog television data does not send the analog television data over the Peripheral Component Interconnect (PCI) bus 20. Instead, as shown in Figure 1 of APA, the analog television data is routed from the TV tuner 18 to the graphics controller 14 and ultimately to the display screen 34. Further, the Office Action's reliance upon the APA ties the Office Action to the many technical disadvantages of the APA as explained at least on page 1, line 9–page 2, line 2 and page 3, line 28–page 5, line 11 in Applicants' Specification. These very disadvantages are overcome by the claimed "sending the decoded digital television data from a local bus of the computer system."

Claims 6 and 38

Claims 6 and 38 are submitted to be allowable as dependent from allowable subject matter.

For the above reasons, the withdrawal of the rejections of claims 6, 8-33, 38 and 48-56 is respectfully requested.

Claims 40-47

Claims 40-47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Drako et al., U.S. Patent No. 5,451,981 and the Admitted Prior Art (APA) of Applicants' Figure 1. These rejections are respectfully traversed.

Regarding claims 40-47, Drako and APA fail to teach or suggest "digital television/local bus interface logic." The Office Action correctly recognizes that Drako does not disclose "digital television/local bus interface logic."[18] The Office Action yet

[17] Col. 2, lns. 61-65.
[18] Paper No. 8, p. 22.

proceeds to rely upon the control circuit 31 in Drako and the TV tuner 18, graphics controller 14, correlogic 10 and graphics controller frame buffer in the APA. None of that constitutes "digital television/local bus interface logic." That the core logic 10 and the TV tuner 18 are shown coupled to the PCI bus 20 does not make the core logic 10 or the TV tuner 18 "digital television/local bus interface logic." The Office Action also appears to ignore altogether that the APA of Applicants' Figure 1 relates to analog television data, not digital television data.

Further regarding claims 40-47, Drako and APA fail to teach or suggest "providing the outgoing digital television data over the local bus." The only bus described in Drako is system bus 24 which carries incoming data to the frame buffer 26, not outgoing data from the frame buffer 26. Further, neither the data in Drako nor the video data in the APA constitutes digital television data.

CONCLUSION

The prior art made of record, but not specifically cited, is not believed to disclose any significant information that is not sufficiently discussed in this Response and Amendment.

It is respectfully submitted that all issues and rejections have been adequately addressed and that all claims are allowable and that the case should be advanced to issuance.

If the Examiner has any questions or wishes to discuss the claims, the Examiner is encouraged to call the undersigned or David R. Clonts at the telephone number indicated below.

Respectfully submitted,

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ATTACHMENT A

Clean Version of Abstract (As of August 2, 2002)

A digital television/local bus interface logic supports handling of digital television (DTV) data with non-tearing. The interface logic provides a dual frame buffer DTV architecture in which a pair of DTV/local bus frame buffers alternate functions: one frame buffer stores incoming DTV data and the other frame buffer stores the outgoing DTV data. When a refresh of a display device reaches a programmed position of the display device, the interface logic determines which frame buffer is being updated by the incoming DTV data. The outgoing DTV data is then read from an opposite frame buffer and transmitted to the display device. The interface logic receives a horizontal sync signal and a vertical sync signal from the graphics controller for monitoring refresh of the display device. The interface logic also provides an architecture for transferring decoded DTV data over a local bus to the graphics controller.

A2 Cancel

ATTACHMENT B

Marked-Up Version of Abstract (As of August 2, 2002)

A digital television/local bus interface logic supports handling of [progressive scan] digital television (DTV) data with non-tearing. The interface logic provides a dual frame buffer DTV architecture in which a pair of DTV/local bus frame buffers alternate functions: one frame buffer stores incoming [progressive scan] DTV data and the other frame buffer stores the outgoing [progressive scan] DTV data. [Incoming DTV data is written to one frame buffer.] When a refresh of a display device reaches a programmed position of the display device, the interface logic determines which frame buffer is being updated by the incoming DTV data. The outgoing DTV data is then read from an opposite frame buffer and transmitted to the display device. [The dual frame buffer DTV architecture insures that the outgoing DTV data to be delivered to the display device includes a whole frame so as to prevent tearing. Outgoing DTV data is synchronized to a refresh rate of a graphics controller coupled to the interface logic.] The interface logic receives a horizontal sync signal and a vertical sync signal from the graphics controller for monitoring refresh of the display device. [The interface logic in effect decouples the refresh rate of the incoming DTV data from the refresh rate of the graphics controller. Non-tearing may therefore be accomplished while optimizing the refresh rate of the outgoing DTV data.] The interface logic also provides an architecture for transferring decoded DTV data over a local bus to the graphics controller. [The interface logic thus eliminates the need for a video port cable between a graphics controller and a television tuner and the need for a non-standard graphics controller video port. Further, the interface logic may be configured to accommodate multiple DTV data streams, permitting scalable picture-in-picture (PIP) functionality.]